



IBM T. J. Watson Research Center

The IBM/MIT PowerPC Project

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PowerPC Architecture Spans Wide Range of Markets



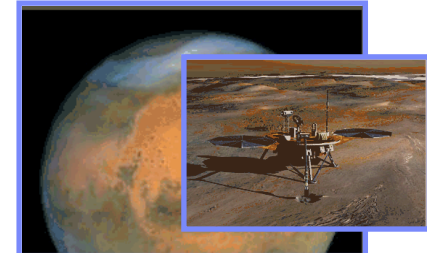
embedded systems



game consoles



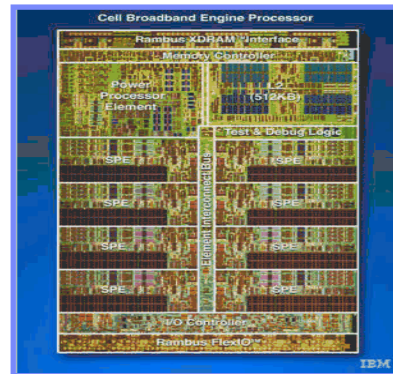
servers



journey to mars



automotives

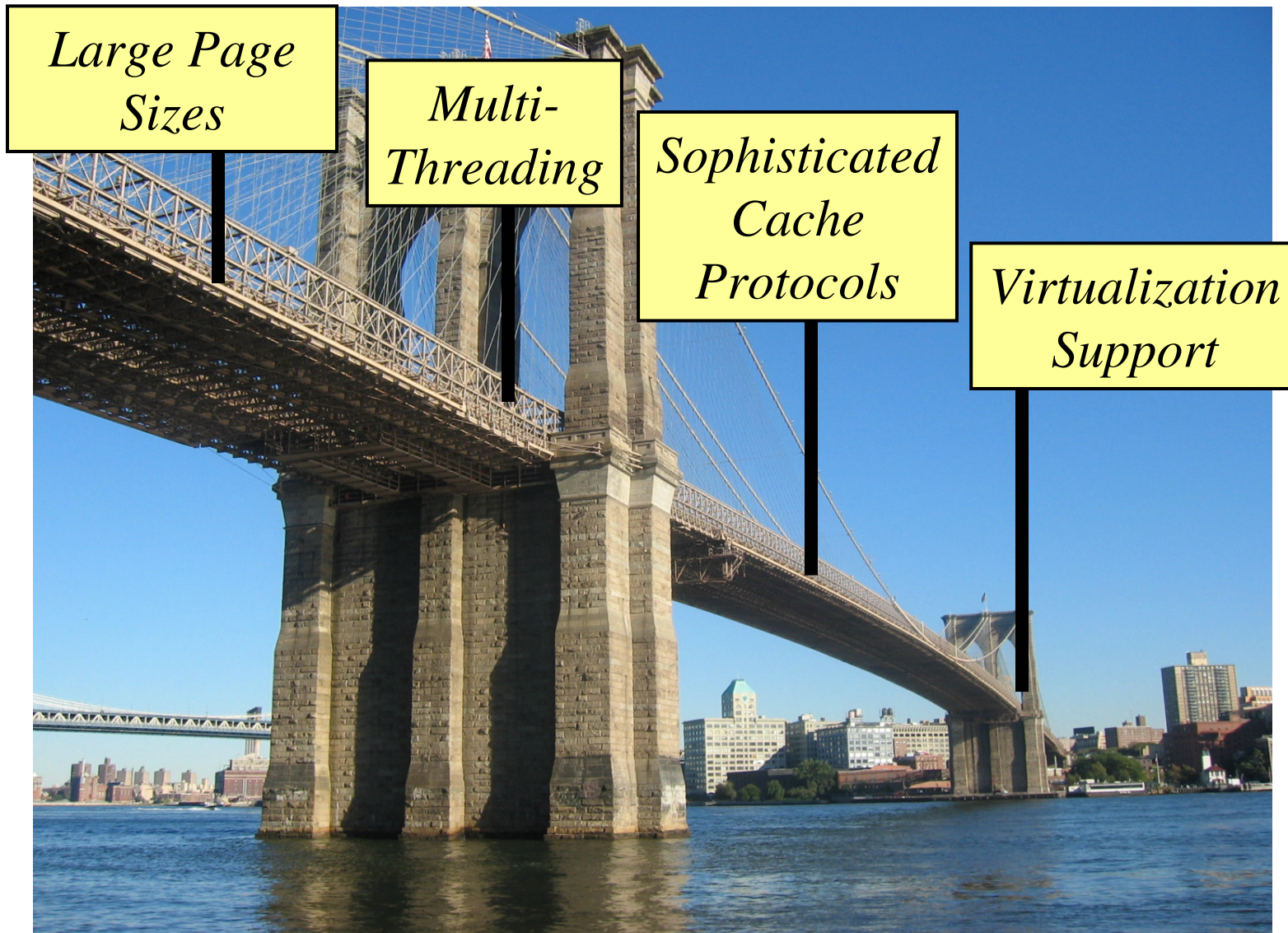


cell broadband engine



super computers (BG/L)

Provide Flexible Support Structures For Software



Our Research Goal and Vision

■ **Goal:**

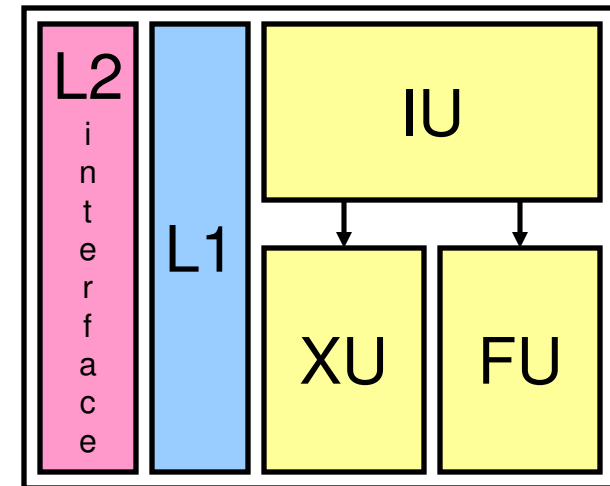
- Promote Power architecture as building block for a wide range of systems and find innovative ways to extend Power architecture with accelerator for specific applications.

■ **Vision:**

- Create an ecosystem to foster Power architecture and ease of its use for system research by the community.

The Basic PowerPC Processor Model

- **Simple in-order pipeline, with standard PowerPC ISA.**
 - Power Instruction Set Architecture Version 2.05 (publicly available from <http://www.power.org>).



- **Some requirements:**

- Support for multiple threads per core.
- Support for multiple cores with shared caches in a node.
- Support for address translation with variable page sizes.
- Support for coherency and synchronization across nodes.

- **Challenges:**

- Facilitate architectural exploration → **Parameterization & Flexibility.**
- *Implement it in one year with a small group of researchers.*
(Began September 2007)

Methodology and Tools

- **Use a high-level hardware description language, **Bluespec SystemVerilog (BSV)**, to create a construct that enables rapid changes to microarchitectures and evaluate their effectiveness for various system and application.**
 - Designed a generic abstraction that controls stages unaware of the number or nature of component stages.
 - Each stage can be designed independently.
 - Stages can be added and removed in a very flexible manner.
 - Pipeline is a vector of stages through which packets of certain type flow.
 - Packet contains information on instruction's operation and its thread.
 - Stage represents operation to be performed on the instruction and could result in status change of the thread.
- **Use **Xilinx** environment to further synthesize the Bluespec generated verilog code onto FPGAs (i.e. Virtex5 LX330) for real-time evaluation and simulation.**

Current Project Status

- **Wrote 10 thousand lines of BSV code**
 - 68 thousand lines of Verilog code
 - 16 thousand slices (30% of available resource of Virtex5 LX330)
[note: without any kind of optimizations]
- **Successfully ran 2.9 millions of Linux boot-up instructions after loading on the C simulation environment of Bluespec.**
- **Successfully integrated the L1 cache model to the processor core and continue on the L2 cache integration.**
- **Investigate the processor stall issues when running on the FPGA platform.**

Acknowledgements

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- **FPGA Prototyping Team**

- Richard Kaufman
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- Kai Schleupen

Thank you!