

# Implementing the LEON3 & GRLIB in RDL

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## 1 Introduction

This document should serve as a repository for our bootcamp plans, and afterwards documentation of our results.

## 2 Proposal

First, and foremost we propose to implement a simple LEON3 system in RDL on the Xilinx XUP board, including multiple components from the Gaisler IP library. We do not propose to write a general set of scripts to generate LEON3 in RDL designs, though we may do so, time permitting.

A key component of this implementation will be a mapping from the AMBA bus to an RDL channel based model. We intend for this to be a general mapping such as might later be automated by tools, and which will apply to any and all AMBA IP blocks.

We intend to be able to run linux on our resulting design.

We will not use the SMP LEON.

## 3 Mapping Leon3 to RDL

Shown in figures 1 and 2 below are the two primary mappings from an AMBA based LEON3 design to RDL. The key difference is that figure 2 avoids the use of the AMBA Bus Interface Units on the IP library blocks. We will likely leave the AMBA interface on the LEON3 itself, as this provides a way to interact with the LEON debugging tools, and we believe separating the LEON from it's Bus Interface Unit to be a prohibitively complex task in the given timeframe.

## 4 Time Line

Friday:  
LEON-3 Core  
AHB RAM or ROM

Timer & Interrupt Controller  
Memory controller  
Debug Interface (Serial)  
AMBA bus interface

Saturday:  
Move to Native RDL (figure 2)  
APB & Bridge  
Serial port  
GPIO  
Ethernet  
Debug the Design

## 5 Conclusion

Figure 1 SimpleMapping

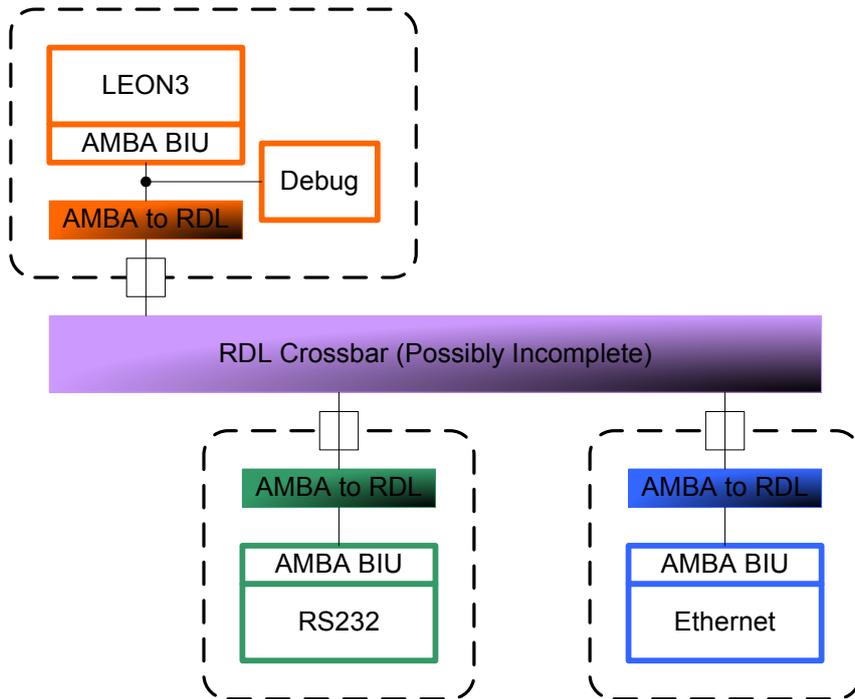


Figure 2 Direct Mapping

