RAMP Blue
Architecture and RDL implementation

RAMP Blue Architecture

Note
- Implemented in EDK
- Currently RAMP blue can have up to eight Microblazes (only four shown)

Tool Flow for RDL design of Ramp Blue

- Write a top_fpga file that instantiate the top unit in unit.v to add non-unit modules and connect to FPGA pins
- Create a new ISE project and add all the generated and copied files
- Copy all black boxes used by EDK into ISE project folder
- Generate Verilog files that instantiate all units, RDL wrappers for each unit & port using RDL compiler
- Write RDL files that instantiate each units
- Write RDL wrapper for each unit to comply with the RDL channel interface, example:

Current implementation (per processor centric)

- Generate a bitfile in ISE
- Compile bootloader
- Run data2mem generate a bit file that initialize bram for each MB with bootloader code
- Download bit