

RAMP Visitor Feedback (January 2007 Retreat)

*** Jiri Gaisler / Gaisler Research

- bc. he's involved in HW design, if we're going to re-use Leon, concerned that we need to think about it, in structured way, such that fixes can be integrated in controlled manner
- every 1-2 months, new version of library (GRLIB?) -- try to keep interface stable, but implementation/parameters might change
- for example, make use of provided scripts (such that that generate compilation order, they are customized for each CAD tool)
- scripts are written in project file format for each CAD tool (i.e. XST project file)
- with a new version of library, using scripts makes it easier to integrate changes to library
- there is an email list (~1200 members), which is a good forum to stay tuned in and asked questions

*** Jaime Moreno / IBM Research

- background on architecture side
- evaluates project as platform for architecture research
- his initial concerns (from start of retreat) were largely taken care of by the end
 - recognition of need to use RDL
 - need to unify independent components
- looking back at last summer, no question there has been a lot of progress, but progress along individual themes
- hoping to see, in a couple months, what we achieve in response to what we (the PIs) have reconized
- once this has been demonstrated, can start to look at further enhancements/contribution from industry

*** Orion Prichard / Altera

- recommends centralizing boards into single farm (to reduce infrastructure costs, enabling time multiplexing, pool hardware resources, etc.)
- for him, seeing fan (in Scott's IBM demo) had same value as physically touching RAMP blue system in front hall

*** Mike Hutton / Altera

- first intro to RAMP, "interesting & exciting project"
- building infrastructure seems vitally important

point 1:

- red flag raised, when he sees "RDL will solve all problems" followed by "we didn't use RDL talk" (or use of Bluespec)
- important to talk to each other before we're deeply invested in one way of

doing things

- particularly important, on this, to re-synch students

point 2:

- see to be emphasis on homogeneous computing model
- once infrastructure developed, would like to see things open up to heterogen. model (he thinks that is an interesting place to go)
- in future going to need to concern selves (i.e. in OS) with heterogeneity

*** Sameh Assad, IBM Research

- 1st retreat, glad to have attended
- reiterate that RDL seems to be central piece in making components work together (or Smash) -- got a bit of a mixed message on this point
 - thought RDL was pre-agreed upon method, though people were unifying on RDL
 - presentations didn't validate that
- RDL is more than a 1 person job, partic. as a "make or break" feature of RAMP
- concerned architects might be intimidated w. FPGAs at outset (as unfamiliar platform) so tools will be important.
- must make it as painless as possible for non-traditional FPGA users to use the platform
- if infrastructure of tools done correctly, it shouldn't matter what platform designs are run on (BEE3, other multi-FPGA system) (should be just a retarget)
- this will be a strength, such that BEE3 is not the RAMP deliverable, but rather the tools

"Are we on track to deliver HW independence model?" (John W.)

- has downloaded and is going to play with RDL
- from presentation, it seems to have promise
- in partic. notion of cycle-accuracy is important, and abstraction of physical from logical channels is valuable

*** Kees Vissers / Xilinx

point 1:

- enjoys talking to people outside of FPGA business
- remarked on progress since last retreat
 - Eric's talk on simulation with multiple layers (FPGA, PPC, Simics):
good talk, good idea
- impressive to see RAMP blue working after early promise of benchmark on 256 microblazes

"What about webcam v. physically present?" (Patterson / John W.)

- good idea

- likes Chuck's idea for BEE3, putting device on back office where it works reliably with
hi-res web-cam is good idea
- in some contexts, i.e. XUP or radio, makes sense to have HW on desk, but
in others, for researchers, visual isn't as important as the reliability of having it up and running
- for San Diego meeting, take XUPs, but remotely log into cabinet/cluster (re-think the added value)

point 2:

- thinks switch from ublaze to Leon is a good idea
- it is not about the ISA, but "can I run an OS, existing binaries on it?"
- interested in SW more than particular processor or ISA

point 3:

- looking at red, blue & white efforts: highly recommends identifying a single person to serve as an architect of the whole system
- without this, design won't automatically coalesce to coherent design
-- Jiri is an excellent example, protecting VHDL programming style, owns the problem
-- Chen is owner of BEE2 signal processing problem
- making a person responsible enables progress
- with a single architect you get a certain style (which may be good or bad), but you also get cohesion

point 4:

- still frustrated that these communities (BWRC & RAMP) are different
- suggests 1/2 or full day overlap in retreats, and carefully select content for that overlap

"What problem does that solve?" (Patterson)

- there is more to computer arch than homogeneous designs, & BWRC folks come at it from the other side
- John W. referred to previous retreat (didn't catch details) w. Jan Rabaey that might have addressed similar situation

*** Paul Hartke / Xilinx

- nice job on demos
- upgraded skillsets are a sign of good things to come
- strongly recommends: documentation & regression suites
-- this is important not only for sanity internally, but for future release of system

*** Scott Lekuch / IBM Research

- 1st RAMP conference, finds it exciting, both the end result and the progression

point 1:

- IBM has vested interest in seeing this work distributed across different platforms
- most directly effects comm. channels between boards (glad to see us

address

PCIE channel)

point 2:

- what IP concerns will we have when we design a custom BEE3 board
- perhaps the solution is just a policy statement
- it is possible he's hypersensitive, but it is important that whatever board we build be as easily distributed as possible
- warning that IP roadblocks can pop up in ways that you don't expect when you don't mean to

"BEE3 -- Berkeley Em. Eng. seems an odd thing for MS to copyright"

(Patterson)

- in Scott's experience, he needs letter from company stating permission to write driver based on datasheet he's already been given
- recognizes that coming from IBM, he might be the *most* sensitive to these issues
- perhaps he's a good litmus test

"Is statement on web about everything being in public domain acceptable?"

(Patterson)

- we seem to still be working things out with MS, keep these issues in mind
- legal restrictions are one thing, but ease of implementation is another (also important, and potentially copyrightable)

point 3:

- centralization (of HW, aggregating HW w. remote access), in addition to other benefits, provides ease of update
- also adds value as point of comparison to system on bench

point 4:

- strongest part of conference for him were demo sessions
- would like to see more of this, even at the expense of presentations
- offers idea of roundtables by area, both for tutorial and technical talks (to encourage more pt. to pt. interactions rather than one to all)

*** Ethan Schuchman / Intel

- more interested in full system prototyping (i.e. RAMP red, architecture for security), than 1000 core machines
- in TM the issues are not scaling to 1k processors, but rather how to write code

- would like to encourage more projects along this line
- don't let optimizing for huge machines get in the way of these "full system" projects

*** Ajit Dingankar / Intel

- 1st RAMP retreat, enjoyed experience
- works on validation tools (not architecture)
- interested in RAMP as bridge to span divide between arch. & validation
- this has been a big problem & RAMP has potential to help with this
- made interesting contacts among participants, and would like to follow through with those to explore the use of RAMP for validation purposes/analyses
- would like to see recognition of non-architecture applications of project
 - recognizes this is longer term and there are immediate short-term tasks

"What do you mean by non-architecture applications?" (John W.)

- for example, validation (architectural & full system)

*** Kai Schleupen / IBM Research

- 2nd RAMP meeting

comment 1:

- last meeting he noticed that Greg alone on RDL was not sufficient, was surprised this hadn't been remedied by now, but is glad to see that we recognize that

comment 2:

- concerned about openness of BEE3
- to use such a platform, you need access to schematics, documentation and tools
- having to go through legal slows things, possibly to the point of losing interest

"Worried about deriving from board or buying a board?" (Patterson)

- buying HW is no problem, but you really need schematic, documentation and firmware info
- need *all* these things to be in public domain

comment 3:

- last meeting he pushed for datacenter formfactor
- has not heard cohesive argument yet about why not to
- blade boards offer the same area
- in standalone environment, non-standard is ok, but once you try to centralize these issues become important
- it also enables mixing of different boards in with BEE3

"How much does a blade rack cost?"

- Universities can get Blade center H for \$2k

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- four power supplies, 2.9kW each, two are redundant, comes standard with 1-
of them

"Quick poll on what people (other companies) think on packaging issue"
(Krstec)

- Jim Keller: board as described seems fine (would rather not have to buy a blade center)
- J. Lockwood: makes sense to pick 1 of three standards: PC, blade, an ATCA chassis
- Konrad: envisions a lot of single board systems, where chassis are unnecessary, perhaps next round, when we know better the uses/market, pay
more attention to formfactor then
- Kai: liked Chuck's plan of having all I/O on one side

comment 4:

- on choice of FPGAs, we've clearly chosen an inexpensive FPGA to keep board price down
- given more money, there are better FPGAs for our purposes

*** Dave Weaver / Sun

- congratulations on coordination of such distributed project
- really enjoyed demos, in partic BEE2 demo with 256 nodes
- also liked seeing Intel and OpenSparc running on FPGAs (he'd never
actually seen demo)
- interesting to see auxiliary technologies tied into project (gives glimpse of bigger picture)
 - asynch logic
 - Martha's talk
- blown away by talk of 1M threads, can see how RAMP is only possible
platform for this

some things that are needed:

- more documentation, including work on RDL'ization and to define interface
- increased coordination & teamwork: share more info to accelerate
production of results
 - proposed retreats/workshops good way to do that
- help Greg w. RDL
- we consumes 2x the coffee as other groups, but significantly less wine!

*** Konrad Lai / Intel

point 1:

- sees many problems with RAMP white, many of which we've identified
 - in partic. unifying the people that are doing the actual work
- important to keep focus on original objective: RAMP to establish

infrastructure for architectural research (red demonstrated some of this possibility, white was to be infrastructure for others)

point 2:

- on BEE3, agrees it is important to get something produced quick for people to use
- on copyright/protection issues, "never to get corporation to say never"
- how about setting it up where MS donates/gifts it to university
 - the credit (tax & otherwise) can motivate people

point 3:

- a lot of architecture research can be done on smaller systems (rather than waiting for 16-board systems)

point 4:

- glad to see us settle on a core that everyone will work on

point 5:

- likes work (James Joe, D. Chiou) in microarchitectural research area

point 6:

- supports all ideas for getting team/grad students together etc.

*** John Lockwood / Stanford, Wash U

(talk w. slides)