OpenSPARC T1 on Xilinx FPGAs – Updates

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RAMP Retreat – January 2008, Berkeley
Agenda

- Quick OpenSPARC Overview
- Progress timeline
- Current Status
  > Solaris Boot
  > Networking
  > Mapping on Virtex 5 parts
  > Availability
- Roadmap
- Q & A
Recap: Big Goals

- Proliferation of OpenSPARC technology
- Proliferation of Xilinx FPGA technology
- Make OpenSPARC FPGA friendly
  > Create reference design with complete system functionality
  > Boot Solaris/Linux on the reference design
  > Open it up
  > Seed ideas in the community

Enable multi-core research
OpenSPARC T1

- SPARC V9 implementation
- Eight cores, four threads each – 32 simultaneous threads
- All cores connect through a 134.4 GB/s crossbar switch
- High BW 12-way associative 3 MB on-chip L2 cache
- 4 DDR2 channels (23 GB/s)
- 70W power
- ~300M transistors
OpenSPARC T1: Some Design Choices

- Simpler core architecture to maximize cores on die
- Caches, DRAM channels shared across cores
- Shared L2 decreases cost of coherence misses significantly
- Crossbar good for b/w, latency, and functional verification
UltraSPARC-T1 Processor Core

- Four threads per core
- Single issue 6 stage pipeline
- 16KB I-Cache, 8KB D-Cache
  - Unique resources per thread
    - Registers
    - Portions of I-fetch datapath
    - Store and Miss buffers
  - Resources shared by 4 threads
    - Caches, TLBs, Execution Units
    - Pipeline registers and DP
- Core Area = 11mm² in 90nm
- MT adds ~20% area to core
Progress Timeline

• RAMP Retreat, July, 2006
  > Sun and Xilinx begin OpenSPARC collaboration

• RAMP Retreat, January 2007:
  > Demonstrated OpenSPARC T1 core mapped on ML411 board (XC4VFX100 FPGA)
    > Ran replays of diagnostic tests

• FCRC/RAMP, June 2007:
  > Demonstrated a stand-alone program running on top of Hypervisor

• RAMP Retreat, January 2008
  > Demonstrated Solaris running (single user) on the ML411 board
Current Status

• Solaris Running on ML411-V4FX100 board
  > Have booted both Solaris 10 and OpenSolaris
  > Run in single-user mode
  > Booted from a RAM disk image
• Networking functional
  > Using polled mode
  > Telnet and FTP are working
  > Close to having interrupts working
• Design is working on Virtex5 board
System Operation

• OpenSPARC T1 core communicates exclusively via cache-crossbar interface (CCX)
  > PCX (processor-to-cache), CPX (cache-to-processor)
  > Glue logic block forwards packets between OpenSPARC core and Microblaze

• Microblaze firmware polls T1 core and system peripherals
  > Services memory and I/O requests
  > Performs address mapping
  > Returns results to the core
  > Maintains coherence of Level-1 caches in OpenSPARC core
Software Stack

- Out-of-the-box operating system installation
- Boots from a virtual disk in RAM which holds the Solaris binaries
- Able to boot either Solaris 10 or OpenSolaris
- Entire software stack is open source
Solaris Boot

```
T1_INFO: cyclic_add: handler 0x125bc68 cyt_interval 0x7735940
Booting to milestone "none".
Requesting System Maintenance Mode
(See /lib/svc/share/README for more information.)
Console login service(s) cannot run

Root password for system maintenance (control-d to bypass):
single-user privilege assigned to /dev/console.
Entering System Maintenance Mode

Jan 4 17:47:31 su: 'su root' succeeded for root on /dev/console
Sun Microsystems Inc. SunOS 5.10 Generic January 2005
# ls
bin       home       platform       system
cbclinks  import     proc           tlb
dev       java       read_time     tmp
devices   kernel     run            usr
dhry      lib        run_commands.sh var
doe       lost+found sbin           workspace
dtextc.dat micro     scde           ws
dungeon   mnt        share           wwss
etc       net        shared
export    opt        src
#_
```
Virtex5 Support

• Using Xilinx ML505 board with same FPGA as BEE3
  > (upgraded 5VLX50T to 5VLX110T)

• Synthesis results (no SPU, 16 TLB entries)
  > 1-thread core: 31475 LUT (45%), 115 BRAM (78%)
  > 4-thread core: 51558 LUT (74%), 115 BRAM (78%)
    > Core only, as synthesized by Synplicity

• Complete system:
  > With MicroBlaze core, 2 UART, ethernet, and DDR2 controller:
    > 1-thread core: 38271 LUT (55%), 128 BRAM (86%)
    > 4-thread core: 58128 LUT (84%), 128 BRAM (86%)
Virtex5 Support

- Single-thread core running on ML505-V5LX110T board
  - Booted Hypervisor
  - Ran stand-alone application program
  - Expect to boot Solaris soon

- Four-thread core placed and routed.
  - Booted Hypervisor
  - Ran stand-alone application program
Demo Details

- ML411 Board
  - Solaris Boot on single-thread OpenSPARC T1
    - Watch Solaris Boot
    - Run ancient text-based adventure game
    - Run Dhrystone MIPS program
Demo Details

- ML505-V5LX110T Board
  - Runs a stand-alone C program on top of Hypervisor.
  - Play the world-famous Dungeon game
Roadmap

• OpenSPARC T1 Release 1.6 planned for 1Q2008
  > EDK project updates
    > MicroBlaze firmware updates for functionality and performance
  > ML505-5VLX110T support
  > Instructions to boot OpenSolaris
  > Complete reference design for 1-thread and 4-thread cores
OpenSPARC momentum

Innovation Happens Everywhere > 6500 downloads

www.opensparc.net
Summary

• OpenSPARC is a complete microprocessor solution
  > Complete simulation environment with regression suites
    > Critical for verifying any changes made to the design
  > EDK environment demonstrated on Virtex4 and Virtex5 FPGAs
  > Choice of 1-thread or 4-thread cores
  > Architectural and simulation models
  > Hypervisor API

• And it's available today!
Team

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