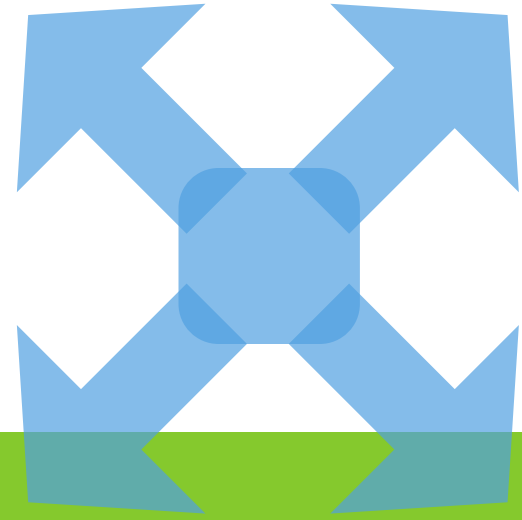
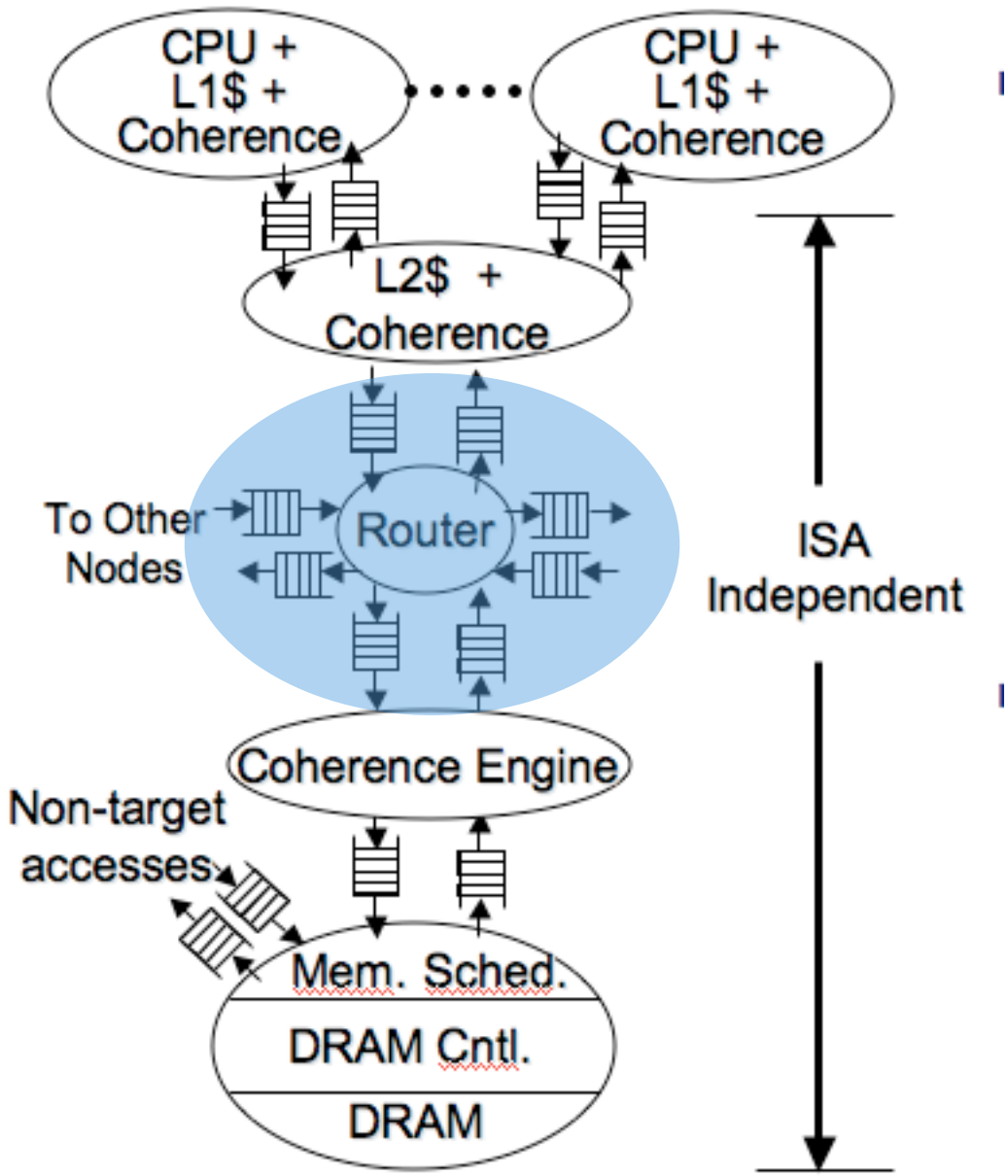


Network Switch

Talking Head: Mark Oskin
Real Work: Andrew Putnam
University of Washington

RAMP White

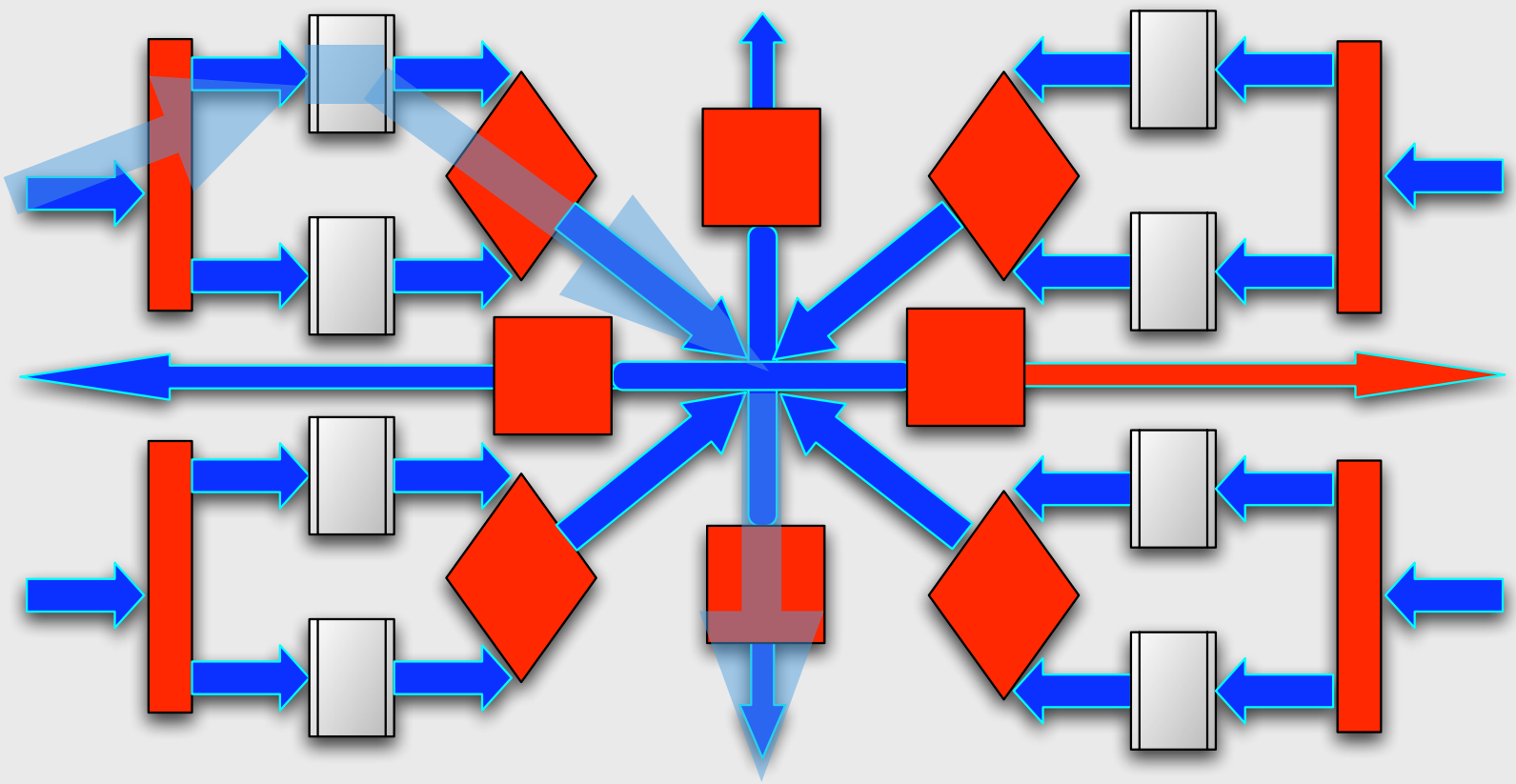

CPU + L1$ + Coherence
CPU + L1$ + Coherence
L2$ + Coherence
To Other Nodes
Router
ISA Independent
Coherence Engine
Non-target accesses
Mem. Sched.
DRAM Cntl.
DRAM

Overview

- Started with Li Shiuan Peh's thesis work... (now at Princeton)
  - "flit reservation router"
  - 5 ports
  - parameterizable width
  - 2 virtual channels
  - Static routing

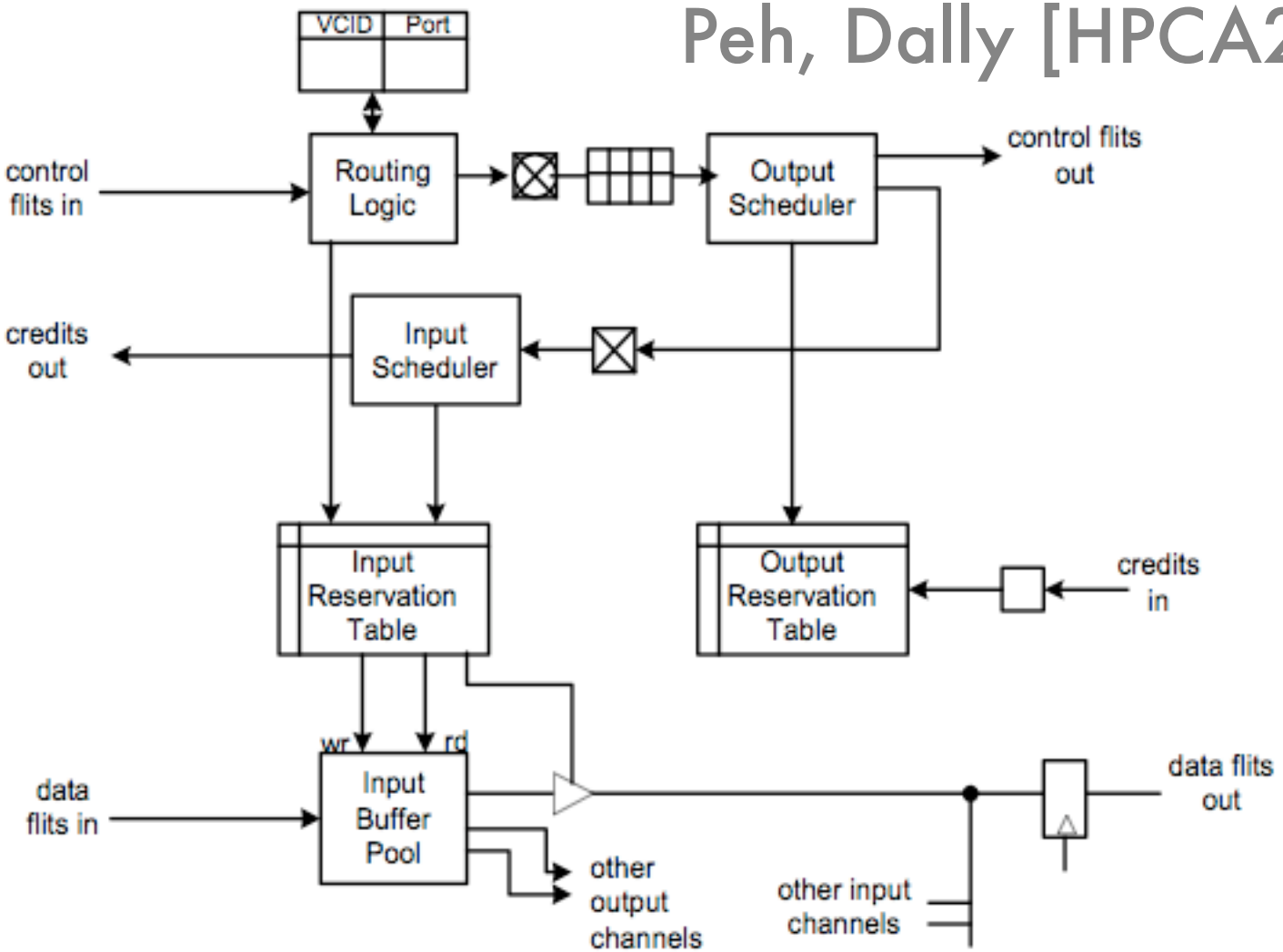
- http://www.princeton.edu/~peh/

Architecture



Scheduling

Peh, Dally [HPCA2000]



Our effort...

- Making it synthesize
  - Significant changes for the tools
  - Switched to synchronous memory
  - Tuning for area, speed
- 8 buffers/port => 3583 slices/10 BRAMS
- 16 buffers/port => 3881 slices/10 BRAMS
- Test benches
- Currently trying to slay the RiDdLer

Where from here…

- You can have the non-RDL version now…
- Maybe Greg and Andrew can mind meld today and finish RDLizing it…
- Future improvements?
  - Andrew is at Xilinx until January 07
  - “More ports is trivial”
  - “Dynamic routing wouldn’t be hard”