Brick and Mortar Silicon Manufacturing

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Declining ASIC Starts

[DataQuest]
Cost of Production

- FPGA
- Standard Cell ASIC
Cost of Production

![Graph showing the cost of production for FPGA, Standard Cell ASIC, and Brick & Mortar Goal. The graph indicates that FPGA has the highest production cost, followed by Standard Cell ASIC, and then the Brick & Mortar Goal, which shows a lower and more stable cost.](www.edn.com)
System on Chip

- Assemble system out of pre-designed components
- Reduce design time
  - In 2004, one engineer costed $392,000 annually [www.design-reuse.com]
- Minimize bugs
  - Initial bugs can cost 50% of revenue [www.design-reuse.com]

PXA27X processor

[www.tomshardware.co.uk]
Brick and Mortar: Assembly

- Bricks -- ASIC chips

  - standard interface

  - implement standard functions

  - i.e., USB, VGA controller, ethernet NIC, PCI bridge, DMA, SRAM, 3DES, JPEG codec, RISC core
Brick and Mortar: Assembly
Brick and Mortar: Assembly
Brick and Mortar: Chip
Brick and Mortar: I/O Pads

- One surface covered with I/O pads
  - 25 um x 25 um / pad
  - 2.5 Gbps / pad
Brick and Mortar: I/O Cap Interconnect

- I/O cap -- ASIC chip implementing inter-brick interconnect
  - packet-switched network
- FPGA-like, island style configurable interconnect
Brick and Mortar: Multiple Brick Sizes
Brick and Mortar: Multiple Brick Sizes

<table>
<thead>
<tr>
<th>Function</th>
<th>Cite</th>
<th>Circuit Area (um²)</th>
<th>Max. Circuit Freq. (MHz)</th>
<th>Min. Perf. (Mbps)</th>
<th>0.25 mm² brick</th>
<th>1.0 mm² brick</th>
<th>4.0 mm² brick</th>
<th>Valid Freq. Range (MHz)</th>
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<td></td>
<td>2,201</td>
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<td>16 - 1370</td>
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</tbody>
</table>
Advantages of Brick and Mortar

- Low manufacturing costs
  - no custom masks
  - small design & verification costs
  - low-cost assembly system (fluidic self assembly)
- ASIC-like degree of circuit integration
- Heterogeneous processes for bricks
- Exclude defective components from assembly
- Leverage process variation for high performance designs
Preliminary Performance Analysis

- Three, 16-way CMP designs
- Only 8% - 36% slowdown relative to ASIC
Why RAMP?

• Once a design has been tested and validated on RAMP platform
  
  • Less costly, per unit, than FPGAs (or boards)
  
  • Higher-speed than FPGAs
Conclusion

• Systems built out of ASIC bricks bonded to an interconnect ASIC

• A viable, low-cost technology if properly architected:
  • appropriate brick functions
  • general, flexible interconnect
  • efficient inter-ASIC communication
Questions & Discussion