QoS-Enforced Communication Channels in Tessellation OS

http://tessellation.cs.berkeley.edu

Gage Eads, John D. Kubiatowicz
Par Lab, UC Berkeley
Communication Channels in Tessellation

- Channels are the inter-cell communication mechanism
  - Channel may be accessed “bare-metal” or via library
  - Cells access services through an RPC-like proxy interface
- Vision: provide performance and security isolation as well
Channel Implementations

- Can implement in hardware...
  - messaging controller, possibly ISA extensions
- ...Or in software
  - Non-blocking buffer on top of shared page
- Shared memory “channels” come with many limitations
  - Channel bandwidth is a function of cache capacity, hierarchy, replacement policy, ...
  - Cells can’t send a notification without kernel assistance
  - Cells can’t stop notification flood without kernel assistance
  - Typically “double-copy”
- Yet they simplify suspend/restart across migration
Hardware Channels Design

Coherence Bus

MP Controller

Queue and Backpressure Logic

Notif?

Channel State
- PID
- Int base
- Rx Q pointers
- QoS allocation

Remaining B/W

Verified Channel Endpoints

Finite State Machine

Message Staging Area

<table>
<thead>
<tr>
<th>Len</th>
<th>Dest</th>
<th>Src</th>
<th>Data[0]</th>
<th>....</th>
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<td>Data[6]</td>
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CPU

D$
Ongoing Work

• Working on two fronts
  – RAMP Gold
    • 64 SPARC core simulator on Virtex-5 FPGA
    • Communication primitives implemented
  – RISC-V multicore processor (work of Par Lab Arch group)
    • Using Chisel HDL, from Bachrach et al., for rapid DSE
    • Exploring energy and performance tradeoffs when coupled with scratchpad memory

Thanks!